

**Homework 02**

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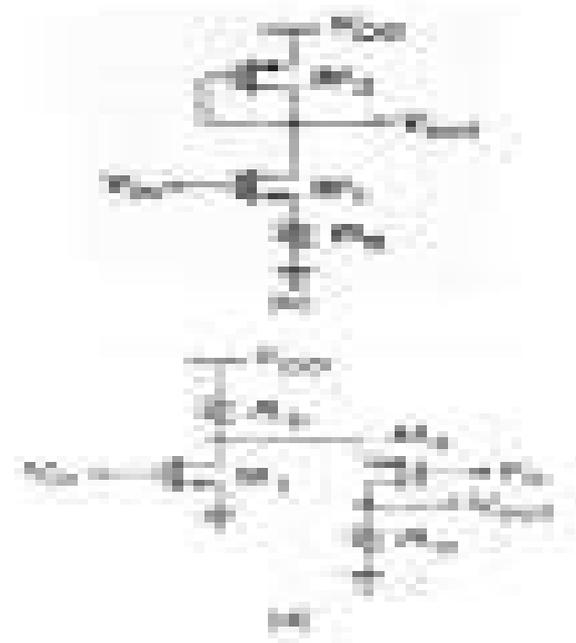
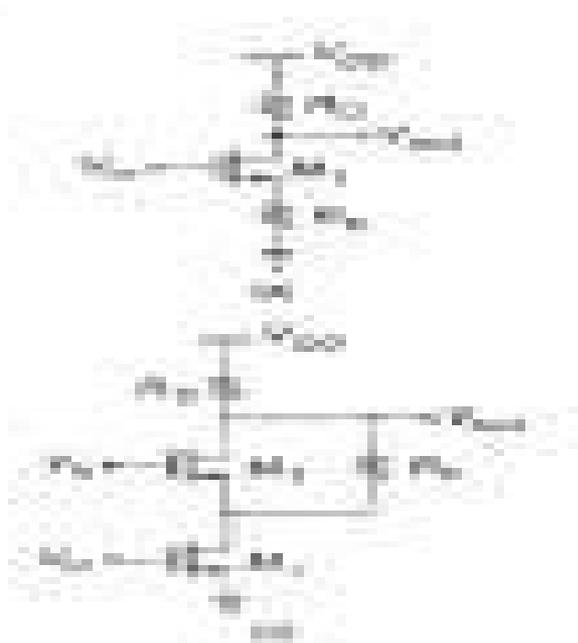
Solve the following problems.

**Problem 1:**

A common-emitter stage is implemented as shown in Fig. 1 and PNPBJ device biased at  $I_C = 1$  mA using  $V_{BE} = 0.7$  V and  $\beta = 100$ . What is the total input and the maximum voltage gain at 100 kHz frequency?

**Problem 2:**

Calculate the input and output voltage gain of the circuit. Assume  $V_{BE} = 0.7$  V and  $\beta = 100$ .



# Analog Integrated Circuit Design Problem Answers

**Yicheng Fang**



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