NII51010-9.1.0

Core Overview

The UART core with Avalon® interface implements a method to communicate serial character streams between an embedded system on an Altera® FPGA and an external device. The core implements the RS-232 protocol timing, and provides adjustable baud rate, parity, stop, and data bits, and optional RTS/CTS flow control signals. The feature set is configurable, allowing designers to implement just the necessary functionality for a given system.

The core provides an Avalon Memory-Mapped (Avalon-MM) slave interface that allows Avalon-MM master peripherals (such as a Nios® II processor) to communicate with the core simply by reading and writing control and data registers.
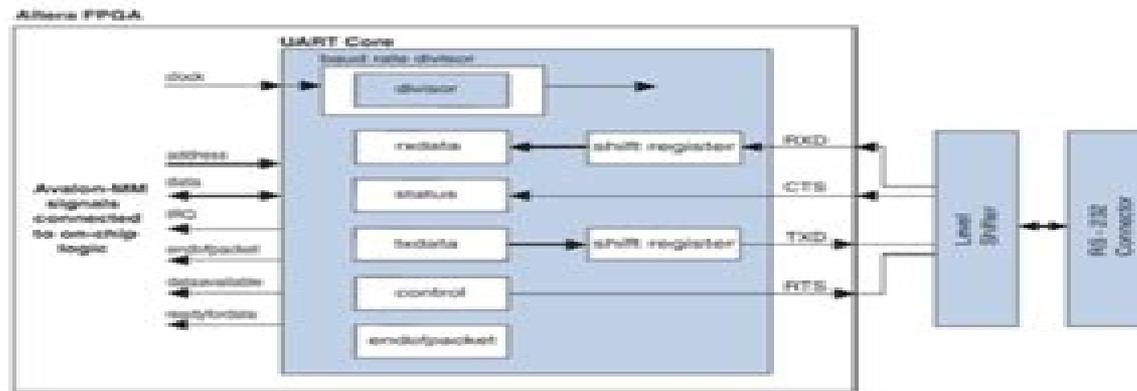
The UART core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. This chapter contains the following sections:

- "Functional Description"
- "Device Support" on page 6–3
- "Instantiating the Core in SOPC Builder" on page 6–3
- "Simulation Considerations" on page 6–7
- "Software Programming Model" on page 6–8

Functional Description

Figure 6–1 shows a block diagram of the UART core.

Figure 6–1. Block Diagram of the UART Core in a Typical System

[6 Uart Core Altera](#)

Tao Wei

6 Uart Core Altera:

This book delves into 6 Uart Core Altera. 6 Uart Core Altera is a vital topic that must be grasped by everyone, ranging from students and scholars to the general public. The book will furnish comprehensive and in-depth insights into 6 Uart Core Altera, encompassing both the fundamentals and more intricate discussions.

1. The book is structured into several chapters, namely:

    - Chapter 1: Introduction to 6 Uart Core Altera
    - Chapter 2: Essential Elements of 6 Uart Core Altera
    - Chapter 3: 6 Uart Core Altera in Everyday Life
    - Chapter 4: 6 Uart Core Altera in Specific Contexts
    - Chapter 5: Conclusion

2. In chapter 1, this book will provide an overview of 6 Uart Core Altera. This chapter will explore what 6 Uart Core Altera is, why 6 Uart Core Altera is vital, and how to effectively learn about 6 Uart Core Altera.
3. In chapter 2, this book will delve into the foundational concepts of 6 Uart Core Altera. This chapter will elucidate the essential principles that need to be understood to grasp 6 Uart Core Altera in its entirety.
4. In chapter 3, this book will examine the practical applications of 6 Uart Core Altera in daily life. This chapter will showcase real-world examples of how 6 Uart Core Altera can be effectively utilized in everyday scenarios.
5. In chapter 4, this book will scrutinize the relevance of 6 Uart Core Altera in specific contexts. This chapter will explore how 6 Uart Core Altera is applied in specialized fields, such as education, business, and technology.
6. In chapter 5, the author will draw a conclusion about 6 Uart Core Altera. This chapter will summarize the key points that have been discussed throughout the book.
    This book is crafted in an easy-to-understand language and is complemented by engaging illustrations. It is highly recommended for anyone seeking to gain a comprehensive understanding of 6 Uart Core Altera.

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Table of Contents 6 Uart Core Altera

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