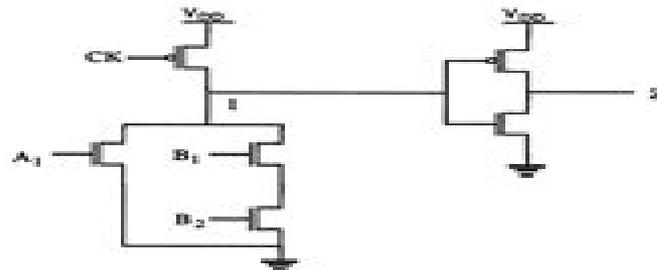


$$\begin{aligned}
 V_{CK} &= 5V, & t < 0 \\
 V_{CK} &= 0V, & 0 \leq t < T_w \\
 V_{CK} &= 5V, & t \geq T_w \\
 V_{DD} &= 5V
 \end{aligned}$$

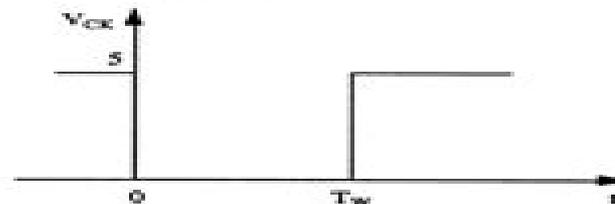
- v) At $t = 0$, the node voltage at I is zero.
 vi) The input voltages at A_1 , B_1 , and B_2 are zero for $0 \leq t \leq T_w$. Find the minimum T_w that allows V_I to reach 2.5 V.

SOLUTION:

(a). The circuit diagram is drawn below:



(b). When the clock signal changes from high to low and A_1 , B_1 , and B_2 are low, node I is charged from 0 to 2.5V through the pMOS transistor.



The transistor first operates in saturation region and then in linear region. Thus,

$$T_w = t_{sat} + t_{lin}$$

When $0 < V_I < 1V$, the transistor is saturated.

$$I = -C \frac{dV_I}{dt}$$

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1. Understanding the eBook Digital Integrated Circuits Solution Manual
 - The Rise of Digital Reading Digital Integrated Circuits Solution Manual
 - Advantages of eBooks Over Traditional Books
2. Identifying Digital Integrated Circuits Solution Manual
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Digital Integrated Circuits Solution Manual
 - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Integrated Circuits Solution Manual
 - Personalized Recommendations
 - Digital Integrated Circuits Solution Manual User Reviews and Ratings
 - Digital Integrated Circuits Solution Manual and Bestseller Lists
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 - Highlighting and Note-Taking Digital Integrated Circuits Solution Manual
 - Interactive Elements Digital Integrated Circuits Solution Manual
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 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Digital Integrated Circuits Solution Manual
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 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Digital Integrated Circuits Solution Manual
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Digital Integrated Circuits Solution Manual
 - Setting Reading Goals Digital Integrated Circuits Solution Manual
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Digital Integrated Circuits Solution Manual
 - Fact-Checking eBook Content of Digital Integrated Circuits Solution Manual
 - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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