

Design of Low Power Efficient CMOS Dynamic Latch Comparator

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Abstract: High performance analog to digital converters (ADC), memory sense amplifiers and Radio Frequency Identification applications, data receivers with less area and power efficient designs has attracted a broad range of dynamic comparators.SAR-ADC is best suited for low power applications where power has a trade-off with speed.Comparator is one of the core components of SAR-ADC that introduces error voltage due to mismatch and consumes large power.This work presents the analysis of various dynamic latch comparators which are there in market and a new comparator has been designed which is optimized to achieve smaller size and less power. The proposed comparators have been designed and simulated using 130nm CMOS 1P2M technology by using mentor graphics tools with a supply voltage of 1V.

Keywords: Analog to digital converters (ADC), CMOS, Dynamic latch comparator, memory sense amplifiers, Radio frequency identification.

I. Introduction

Due to high-speed, less-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators[1] are very attractive for many applications such as high-performance analog-to-digital converters (ADC's), memory sense amplifiers (SAs) and data receivers. A small input-voltage difference is converted into full-scale digital level in a short time by using the positive feedback mechanism with one pair of back-to-back cross-coupled inverters (latch) in conventional dynamic latched comparators. However, the accuracy and the performance of the dynamic latched comparators is restricted by the random offset voltage which results from device mismatches such as threshold voltage V_{th} , current factor $\beta (= \mu C_{ox} W/L)$, and internal-parasitic/external load capacitance mismatches [2],[3],[4]. The most important design parameter in designing dynamic latched comparator is offset voltage[5],[6] which shows a large effect on performance of the comparator. In Fig. 1, shows the block diagram of high speed comparator which consists of pre-amplifier and regenerative latch stage. The pre amplifier stage is used to decrease the latch offset voltage and it can also amplify a small input voltage difference to a large output voltage. This large output voltages to overcome the latch offset voltage which in turn reduces the kickback noise [7]. There will be large static power consumption for large bandwidths because of the pre-amplifier stage and the intrinsic gain also reduced due to the reduction of the drain-to-source resistance (r_{ds}), due to the continuous technology scaling [8]. Therefore, for the high-performance CMOS applications, a dynamic comparator without pre-amplifier stage is highly desirable. The conventional comparators suffer a lot of accuracy issues like random offset errors and internal parasitic/external load capacitances mismatches [2],[3],[4]. To overcome this inaccuracy issues and to improve the performance dynamic latch based comparators without pre-amplifier stage are preferred [7]. For an analog to digital converter with a feature of high-performance, a comparator without the pre-amplifier is preferred since it suffers from high static power dissipation [9].



Figure 1 Typical block diagram of a high speed voltage comparator.

In this paper the sections are considered as follows: Section II offers an overview of the dynamic latch comparators and also discuss about their advantages and downsides, and Section III describes the proposed

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