

Core Overview

The UART core with Avalon® interface implements a method to communicate serial character streams between an embedded system on an Altera® FPGA and an external device. The core implements the RS-232 protocol timing, and provides adjustable baud rate, parity, stop, and data bits, and optional RTS/CTS flow control signals. The feature set is configurable, allowing designers to implement just the necessary functionality for a given system.

The core provides an Avalon Memory-Mapped (Avalon-MM) slave interface that allows Avalon-MM master peripherals (such as a Nios® II processor) to communicate with the core simply by reading and writing control and data registers.

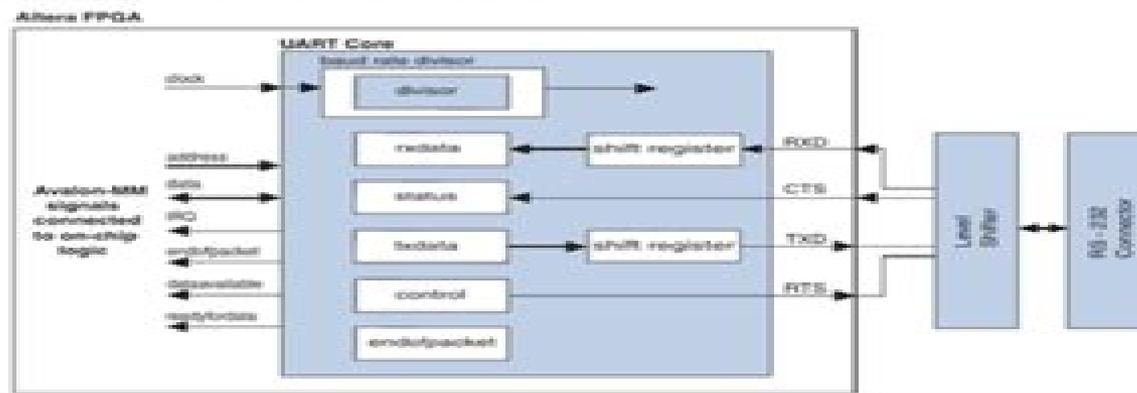
The UART core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. This chapter contains the following sections:

- "Functional Description"
- "Device Support" on page 6-3
- "Instantiating the Core in SOPC Builder" on page 6-3
- "Simulation Considerations" on page 6-7
- "Software Programming Model" on page 6-8

Functional Description

Figure 6-1 shows a block diagram of the UART core.

Figure 6-1. Block Diagram of the UART Core in a Typical System



6 Uart Core Altera

Julia Schneider



6 Uart Core Altera:

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