Modular Verification of Timed Circuits Using Automatic Abstraction

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***Abstract*—The major barrier that prevents the application of formal verification to large designs is state explosion. This paper presents a new approach for verification of timed circuits using automatic abstraction. This approach partitions the design into modules, each with constrained complexity. Before verification is applied to each individual module, irrelevant information to the behavior of the selected module is abstracted away. This approach converts a verification problem with big exponential complexity to a set of sub-problems, each with small exponential complexity. Experimental results are promising in that they indicate that our approach has the potential of completing much faster while using less memory than traditional flat analysis.**

***Index Terms*—timed circuits, modular verification, abstraction.**

I. Introduction

In order to continue to produce circuits of increasing speed, designers are considering aggressive circuit styles such as self-resetting or delayed-reset domino circuits. These circuit styles can achieve a significant improvement in circuit speed as demonstrated by their use in a gigahertz research microprocessor (guTS) at IBM [1]. Designers are also considering asynchronous circuits due to their potential for higher performance and lower power consumption as demonstrated by the RAPPID instruction length decoder designed at Intel [2]. This design was 3 times faster while using only half the power of the synchronous design. The correctness of these new *timed circuit* styles is highly dependent upon their timing parameters, so extensive timing verification is necessary during the design process. Unfortunately, these new circuit styles cannot be efficiently and accurately verified using traditional static timing analysis methods. This lack of efficient analysis tools is one of the reasons for the lack of mainstream acceptance of these circuit styles.

In [3], a hierarchical approach to verification based on trace theory is proposed for the analysis of speed-independent circuits. In this approach, a model of a circuit at one level is regarded as the implementation of the model at the higher level and as the specification of the model at the lower level. The model at the higher level is more abstract and has less implementation details. A circuit is a correct implementation if it conforms to its specification. Trace theory has proved to be an excellent model for verifying circuits, and it is trace theory that this paper utilizes to justify its approach.

In [4], [5], trace theory is extended with a representation where time is modeled as multiples of a discretization constant. Unfortunately, the state space explodes if the delay ranges are large and the discretization constant is set small enough to ensure exact exploration of the state space. In [6], timed automata are introduced to model the behavior of real-time systems. It provides a simple and general way to annotate state-transition graphs with timing constraints using a finite number of real-valued *clocks*. Although this approach eliminates the need to discretize time, the number of timed states is dependent on the size of the delay ranges and the number of concurrently enabled clocks which can quickly explode for even relatively small systems. Representing possible clock values with convex polygons, or zones, [7] alleviates this problem in practice. The zone based representation is the one used by most modern timing verifiers such as ATACS [8]–[10], VINAS-P [11], ORBITS [12], [13], KRONOS [14], and UPPAAL [15]. One feature common to these tools is that they require state space exploration which can explode even for modest size examples.

There do exist many methods and approaches to address the state explosion problem. In [16], [17], the state space of a transition system is represented symbolically using Bryant's *ordered binary decision diagram* [18]. The symbolic approach has been shown to be capable of representing systems with more than 10^{20} states. There has been some success at the verification of timed systems using binary decision diagrams [19], [20]. Asynchronous systems consist of concurrent processes without a global synchronizing clock. State explosion is particularly serious for asynchronous systems because all possible interleavings among concurrently executed events need to be explored. A number of techniques have been proposed to minimize the number of interleavings that are explored, including stubborn sets [21], partial orders [22], and unfoldings [23]. There has also been some success at applying partial orders to formal timing verification [11], [24]. Although the approaches described above have been successful in verifying systems with increased sizes, many realistic systems are still too large to be handled.

In practice, circuits often have inherent modular structures. Compositional verification methods based on *assume-guarantee reasoning* [25]–[27], exploit the modular structure of circuits. Verifying a circuit component in this approach necessitates behavioral assumptions on connecting components to reduce complexity in the model. The assumptions must later be discharged as part of the correctness proof for connecting

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Modular Verification Of Timed Circuits Using Automatic:

Automated Technology for Verification and Analysis Susanne Graf,Wenhui Zhang,2006-10-11 This book constitutes the refereed proceedings of the Third International Symposium on Automated Technology for Verification and Analysis ATVA 2006 held in Beijing China in October 2006 The 35 revised full papers presented together with abstracts of three keynote papers were carefully reviewed and selected from 137 submissions Modular Synthesis and Verification of Timed Circuits Using Automatic Abstraction Hao Zheng,2001 *Model Checking Software* Alastair Donaldson,David Parker,2012-07-18 This book constitutes the thoroughly refereed proceedings of the 19th International SPIN workshop on Model Checking Software SPIN 2012 held in Oxford UK in July 2012 The 11 revised full papers presented together with 5 tool papers and 4 invited talks were carefully reviewed and selected from 30 submissions The papers are grouped in topical sections on model checking techniques parallel model checking case studies model checking for concurrency and tool demonstrations

Formal Modeling and Analysis of Timed Systems Kim G. Larsen,Peter Niebert,2004-04-08 This book constitutes the thoroughly refereed post proceedings of the First International Workshop on Formal Modeling and Analysis of Timed Systems FORMATS 2003 held in Marseille France in September 2003 The 19 revised full papers presented together with an invited paper and the abstracts of two invited talks were carefully selected from 36 submissions during two rounds of reviewing and improvement All current aspects of formal method for modeling and analyzing timed systems are addressed among the timed systems dealt with are timed automata timed Petri nets max plus algebras real time systems discrete time systems timed languages and real time operating systems **10th International Symposium on Asynchronous Circuits and Systems** ,2004 IEEE Computer Society Order Number P2133 T p verso **Asynchronous Circuit Design for VLSI Signal Processing** Teresa H. Meng,Sharad Malik,2011-06-27 Asynchronous Circuit Design for VLSI Signal Processing is a collection of research papers on recent advances in the area of specification design and analysis of asynchronous circuits and systems This interest in designing digital computing systems without a global clock is prompted by the ever growing difficulty in adopting global synchronization as the only efficient means to system timing Asynchronous circuits and systems have long held interest for circuit designers and researchers alike because of the inherent challenge involved in designing these circuits as well as developing design techniques for them The frontier research in this area can be traced back to Huffman s publications The Synthesis of Sequential Switching Circuits in 1954 followed by Unger s book Asynchronous Sequential Switching Circuits in 1969 where a theoretical foundation for handling logic hazards was established In the last few years a growing number of researchers have joined force in unveiling the mystery of designing correct asynchronous circuits and better yet have produced several alternatives in automatic synthesis and verification of such circuits This collection of research papers represents a balanced view of current research efforts in the design synthesis and verification of asynchronous systems *Automata, Languages and Programming* Thomas Ottmann,1987-07-08 This volume contains the proceedings of the 14th International Colloquium on Automata Languages and Programming organized by the European Association for Theoretical Computer Science EATCS and held in Karlsruhe July 13 17 1987 The papers report on original research in theoretical computer science and cover topics such as algorithms and data structures automata and formal languages computability and complexity theory semantics of programming languages program specification transformation and verification theory of data bases logic programming theory of logical design and layout parallel and distributed computation theory of concurrency symbolic and algebraic computation term rewriting systems cryptography and theory of robotics The authors are young scientists and leading experts in these areas *25 Years of Model Checking* Orna Grumberg,Helmut Veith,2008-06-17 This Festschrift volume published in celebration of the 25th Anniversary of Model Checking features papers based on talks at the symposium 25 Years of Model Checking 25MC which was part of the 18th International Conference on Computer Aided Verification **Dissertation Abstracts International** ,2003 **Logics of Programs, Workshop, Carnegie Mellon University, Pittsburgh, PA, June 6-8, 1983** Edmund Clarke,Dexter Kozen,1984 Computer-aided Verification ,2001 *Automated Design of Signal Acquisition Modules* Monte Frank Mar,1993 *Automatic Synthesis of CMOS Digital/analog Converters* Robert McKinstry Robinson Neff,1995 **XI Brazilian Symposium on Integrated Circuit Design** Marcelo Lubaszewski,Vladimir Castro Alves,1998 Topics in this book on integrated circuit design include hardware software codesign of embedded systems the ALFA HUERTA project rapid prototyping digital testing and digital design *Proceedings of the ... Custom Integrated Circuits Conference* ,1986 **VLSI 91** Arne Halaas,Peter B. Denyer,1992 The major problem in VLSI is really the control of complexity The hardest part is the control of autonomous yet interacting processes We do not yet have satisfactory techniques for handling that sort of thing but I think the techniques we need to develop are independent of whether you are programming or designing the chip Sidney Michaelson Initiator of the IFIP Working Group on VLSI This proceedings dedicated to the late Prof Sidney Michaelson who ten years ago established this IFIP Working Group reflects the continuing interest in improving design tools and the wide range of engineering concerns surrounding the effective exploitation of VLSI Digest of Technical Papers ,1987 **CONCUR '92** Walter Rance Cleaveland,1992 This book contains a selection of research papers describing recent advancesin the theory of concurrent systems and their applications The papers were all presented at the CONCUR 92 conference which has emerged as the premiere conference on formal aspects of concurrency The authors include such prominent researchers as R Milner A Pnueli N Lynch and V R Pratt The results represent advances in the mathematical understanding of the behavior of concurrent systems topics covered include process algebras models of true concurrency compositional verification techniques temporal logic verification case studies models of probabilistic and real time systems models of systems with dynamic structure and algorithms and decidability results for system analysis A key feature of CONCUR is its breadth in one volume it presents a snapshot of the state of the art in concurrency theory Assuch it is

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